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| **Batch :** |  |

**Experiment No: 8**

**Title:** Arithmetic Logic Unit

**Estimated time to complete this experiment:**2 hours

**Objective:**

1.Understanding behaviour of arithmetic logic unit from working module and the module designed by the student as part of the experiment

2. Designing an arithmetic logic unit for given parameter

**Books/ Journals/ Websites referred:**

Books:

1. Digital Logic and Computer Design - M. Morris Mano. Pearson Education - Prentice Hall.
2. Digital Principles Foundation of Circuit Design and Application - Arun Kumar Singh. New Age Publishers.
3. The Art of Electronics - Paul Horowitz and Winfield Hill (1989). Cambridge University Press
4. Modern Dictionary of Electronics - Rudolf F. Graf (1999). Newnes

Web Sites:

* [http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/Comb/ adder.html](http://www.cs.umd.edu/class/spring2003/cmsc311/Notes/Comb/adder.html)
* <http://en.wikipedia.org/wiki/Adder_(electronics)>
* [NPTEL (e-learning courses from IITs and IISC)](http://nptel.iitm.ac.in/courses.php?disciplineId=106)

**Requirements:** Virtual simulator.

**Components:**

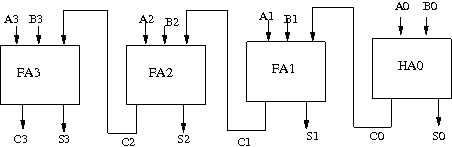
To build any 4 bit ALU, we need :

1. AND gate, OR gate, XOR gate

2. Full Adder,

3. 4-to-1 MUX<

4. Wires to connect

Circuit Diagram:

**Procedure:**

1.Start the simulator as directed.This simulator supports 5-valued logic.

2.To design the circuit we need 4 1-bit ALU, 11 Bit switch (to give input,which will toggle its value with a double click), 5 Bit displays (for seeing output), wires

3.. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette. Pin numbering starts from 1 and from the bottom left corner (indicating with the circle) and increases anticlockwise

4.. For 1-bit ALU input A0 is in pin-9,B0 is in pin-10, C0 is in pin-11 (this is input carry), for selection of operation, S0 is in pin-12, S1 is in pin-13, output F is in pin-8 and output carry is pin-7

5 .Click on the 1-bit ALU component (in the Other Component drawer in the pallet) and then click on the position of the editor window where you want to add the component (no drag and drop, simple click will serve the purpose), likewise add 3 more 1-bit ALU (from the Other Component drawer in the pallet), 11 Bit switches and 5 Bit Displays (from Display and Input drawer of the pallet,if it is not seen scroll down in the drawer), 3 digital display and 1 bit Displays (from Display and Input drawer of the pallet,if it is not seen scroll down in the drawer)

6. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components. Connect the Bit switches with the inputs and Bit displays component with the outputs. After the connection is over click the selection tool in the pallete.

7. See the output, in the screenshot diagram we have given the value of S1 S0=11 which will perform add operation and two number input as A0 A1 A2 A3=0010 and B0 B1 B2 B3=0100 so get output F0 F1 F2 F3=0110 as sum and 0 as carry which is indeed an add operation.you can also use many other combination of different values and check the result. The operations are implemented using the truth table for 4 bit ALU given in the theory

**Conclusion:**  An ALU is a basic building block in many types of computing circuits, including the CPU of computers, FPUs and GPUs. A single CPU, GPU, FPU may contain multiple ALUs.

In many designs, the ALU also has status inputs or outputs, or both, which convey information about a previous operation or the current operation, respectively, between the ALU and external [status registers](https://en.wikipedia.org/wiki/Status_register).

**Real Life Application:**

1. Perform Arithmetic Operation
2. Multiple Precision arithmetic
3. Complex Operation

**Post Lab Questions:**

Q. Describe with a schematic diagram, how the ALU is connected to the processor registers through common bus?

Q. Why are accumulators used in ALU?

Q. What are the rules for detecting overflow in 2’s compliment sum?